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To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

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Subject: Serial No. 09/755,572 01/08/01

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NOVEL METHOD OF BODY CONTACT FOR
SOI MOSFET

Grp. Art Unit:

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

The SOI technology is discussed in "Silicon Processing for the VLSI Era", Vol. 2, by S. Wolf, Lattice Press, Sunset Beach, CA, c. 1990, pp. 66-67.

U.S. Patent 5,874,328 to Liu et al., "Reverse CMOS Method for Dual Isolation Semiconductor Device", discloses trench isolation through a source/drain region.

U.S. Patent 5,504,033 to Bajor et al., "Method for Forming Recessed Oxide Isolation Containing Deep and Shallow Trenches", discloses a process for forming both deep and shallow trenches in a SOI device.

The following two U.S. Patents disclose an SOI device having a shallow trench isolation (STI) formed entirely through the silicon to the oxide layer:

1) U.S. Patent 6,063,652 to Kim, "Silicon-On-Insulator Semiconductor Device Improving Electrostatic Discharge Protection Capability and Fabrication Method Thereof".

2) U.S. Patent 5,591,650 to Hsu et al., "Method of Making a Body Contacted SOI MOSFET".

U.S. Patent 5,674,760 to Hong, "Method of Forming Isolation Regions in a MOS Transistor Device", discloses an isolation structure.

U.S. Patent 5,930,605 to Mistry et al., "Compact Self-Aligned Body Contact Silicon-On-Insulator Transistors", discloses a Schottky diode connection between the body and one of the source/drain regions.

Sincerely,

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